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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,893	08/21/2003	Young-Hwan Yun	SEC.1061	6402

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EXAMINER	
YOUNG, BRIAN K	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 02/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/644,893	YUN ET AL.	
	Examiner	Art Unit	
	Brian Young	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10-20* is/are allowed.

6)☒ Claim(s) *1* is/are rejected.

7)☒ Claim(s) *2-9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Yang et al. Yang et al disclose (fig.4) an image signal processing circuit comprising an analog integrated circuit (CMOS image sensor circuit 200) having a first input terminal that receives a first-level analog signal (the image sensor diode connected to node N1) during a first active period (before RESET input) of a first switching signal and a second input terminal that receives a time varying reference (signal capacitor CD), and an input circuit being coupled to data (Vinv) to receive an analog signal corresponding to image charges of an image input element during a second active period of the first switching signal, an inverter circuit (see Vinv) that inverts and amplifies (Vamp) an output of said analog integrated circuit in response to an activated enable signal, and an output circuit that generates a digital word (Bit ADC to Digital Signal Processor) indicative of a time period defined by a start signal and an end signal corresponding to a transition of an output of said inverter circuit, wherein the enable signal is deactivated between an end point of the first active period and an end point of the second active period of the first switching signal.

Yang et al recite (col.7, lns.20-37) "as illustrated in FIG. 4, a low-bit resolution and high spatial resolution ***CMOS area image sensor 200*** is provided for operation of more than 1-bit but less than 6-bits. A more detailed illustration of the connection between the pixels and the column processors is illustrated in FIG. 5. This embodiment differs from the embodiment illustrated in FIG. 1 in that the sense amplifier connected to the bitline in FIG. 1 is now replaced with a low-bit (i.e., less than 6 bits) ADC, which converts analog image signal into digital image signal. ***Preferably, analog dithering is performed by changing a reset value of the pixel as described previously in this specification and by modifying the ADC quantization levels of the low-bit ADC.*** For example, for a low bit single slope ADC, analog dithering with the ADC may also be performed by introducing an offset in the starting voltage of the RAMP voltage or the start time of the counter. Analog dithering can also be performed with other low bit ADC architectures such as flash ADC, successive comparison ADC, successive approximation ADC, and algorithmic ADC".

3. Claims 2-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. Claims 10-20 are allowed.

5. The following is an examiner's statement of reasons for allowance: a sensor that provides a sensor signal at a sensor output terminal; ***a sampling circuit having a first switch coupled between the sensor output terminal and a first electrode of a first capacitor, and a second switch coupled between a time varying reference signal***

and a first electrode of a second capacitor, wherein second electrodes of the first and second capacitors are coupled to an output terminal of said sampling circuit, and wherein the first and second switches are respectively controlled by first and second switching signals; switches are respectively controlled by first and second an inverter circuit that inverts and amplifies a sampled signal provided at the output terminal of said sampling circuit, responsive to an activated enable signal; and an output circuit that generates a digital word responsive to an output of said inverter circuit, has not bee shown in the prior art.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Yadid-Pecht et al disclose an imaging device, comprising:
a substrate formed of a semiconductor material;
an image detector array, having a plurality of pixel circuits formed on said substrate, each pixel circuit generating a pixel signal indicative of a pixel of an image;
a first signal buffer, formed on said substrate and coupled to respectively store pixel signals from a first group of said pixel circuits; a second signal buffer, formed on said substrate and coupled to respectively store pixel signals from a second group of said pixel circuits, wherein said second group is displaced from said first group by a predetermined number of pixel circuits; and a control circuit coupled to control said

image detector array and said first and second signal buffers, said control circuit controlling reading out pixel circuits into said first buffer with a first integration time and controlling reading out pixel circuits into said second buffer with a second integration time different than said first integration time, said first and second buffers storing two different signals with two different integration times for each pixel circuit, wherein said first and second integration times have a difference which depends on said predetermined number of pixel circuits between said first and second groups, wherein said control circuit is adapted to select signals with said first integration time from a first group of pixel circuits and signals with said second integration time from a second group of pixel circuits to form said single frame where said first group of pixel circuits receive less light than said second group of pixel circuits.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Young whose telephone number is 571-272-1816. The examiner can normally be reached on Mon-Fri 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian Young
Primary Examiner
Art Unit 2819

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